# N-CHANNEL ENHANCEMENT MODE VERTICAL DMOS FET

**ZVN4424A/C** 

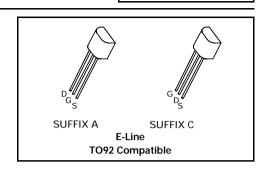
### ISSUE 3 - August 1994

#### **FEATURES**

- \* Compact E-LINE (TO92 style) package
- \* 240 Volt BV<sub>DS</sub>
- \*  $R_{DS(on)}$ =4.3 $\Omega$  Typical at  $V_{GS}$ =2.5V
- Low threshold
- Fast switching

### **APPLICATIONS**

- \* Earth recall and dialling switches
- Electronic hook switches
- \* Battery powered equipment
- \* Telecoms and high voltage dc-dc converters



### ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V <sub>DS</sub>	240	V
Continuous Drain Current at T <sub>amb</sub> =25°C	I <sub>D</sub>	260	mA
Pulsed Drain Current	I <sub>DM</sub>	1.5	А
Gate Source Voltage	V <sub>GS</sub>	± 40	V
Power Dissipation at T <sub>amb</sub> =25°C	P <sub>tot</sub>	750	mW
Operating and Storage Temperature Range	T <sub>j</sub> :T <sub>stg</sub>	-55 to +150	°C



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FIG. 8 Typical Gate Charge vs.

Gate-Source Voltage

### TYPICAL CHARACTERISTICS

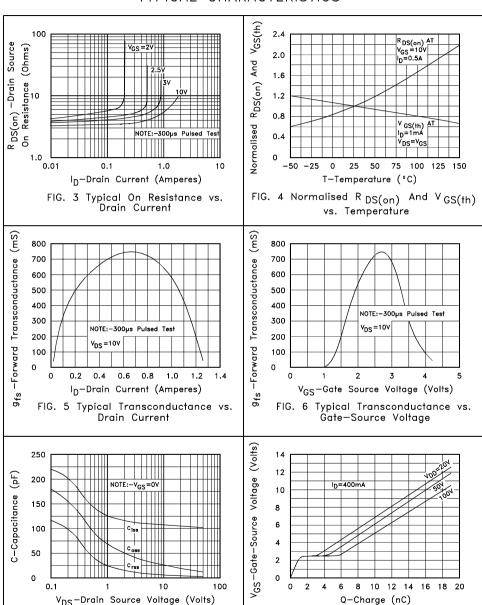


FIG. 7 Typical Capacitance vs.

Drain-Source Voltage

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## ELECTRICAL CHARACTERISTICS (at T<sub>amb</sub> = 25°C unless otherwise stated).

PARAMETER	SYMBOL	MIN.	TYP	MAX.	UNIT	CONDITIONS.	
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	240			V	I <sub>D</sub> =1mA, V <sub>GS</sub> =0V	
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	0.8	1.3	1.8	V	$I_D=1mA$ , $V_{DS}=V_{GS}$	
Gate-Body Leakage	I <sub>GSS</sub>			100	nA	$V_{GS}=\pm 40V$ , $V_{DS}=0V$	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			10 100	μ <b>Α</b> μ <b>Α</b>	V <sub>DS</sub> =240 V, V <sub>GS</sub> =0 V <sub>DS</sub> =190 V, V <sub>GS</sub> =0V, T=125°C	
On-State Drain Current	I <sub>D(on)</sub>	0.8	1.4		Α	V <sub>DS</sub> =10 V, V <sub>GS</sub> =10V	
Static Drain-Source On-State Resistance	R <sub>DS(on)</sub>		4 4.3	5.5 6	$\Omega$ $\Omega$	V <sub>GS</sub> =10V,I <sub>D</sub> =500mA V <sub>GS</sub> =2.5V,I <sub>D</sub> =100mA	
Forward Transconductance (1) (2)	g <sub>fs</sub>	0.4	0.75		S	V <sub>DS</sub> =10V,I <sub>D</sub> =0.5A	
Input Capacitance (2)	C <sub>iss</sub>		110	200	pF	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, f=1MHz	
Common Source Output Capacitance (2)	C <sub>oss</sub>		15	25	pF		
Reverse Transfer Capacitance (2)	C <sub>rss</sub>		3.5	15	pF		
Turn-On Delay Time (2)(3)	t <sub>d(on)</sub>		2.5	5	ns		
Rise Time (2)(3)	t <sub>r</sub>		5	8	ns	V <sub>DD</sub> ≈50V, I <sub>D</sub> =0.25A, V <sub>GEN</sub> =10V	
Turn-Off Delay Time (2)(3)	t <sub>d(off)</sub>		40	60	ns		
Fall Time (2)(3)	t <sub>f</sub>		16	25	ns		

- (1)\*Measured under pulsed conditions. Pulse width=300 $\mu$ s. Duty cycle  $\leq$ 2% (2)Sample Test
- (3) Switching times measured with  $50\Omega$  source impedance and >5ns rise time on pulse generator

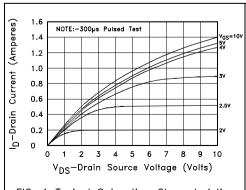
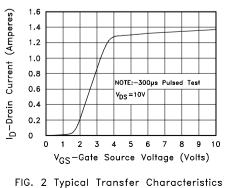
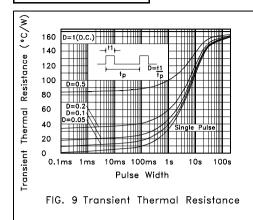
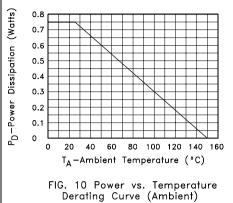


FIG. 1 Typical Saturation Characteristics



# **ZVN4424A/**C





#### SPICE PARAMETERS

\*ZVN4424 MODEL LAST REVISION 1/94

\*

.SUBCKT ZVN4424 30 40 50

\* NODES: DRAIN GATE SOURCE

M1 30 20 50 50 MOD1 L=1 W=1

RG 40 20 200

RL 30 50 240E6

D1 50 30 DIODE1

.MODEL MOD1 NMOS VT0=1.25 RS=2.34 RD=1.634 IS=1E-15 KP=5.319

+CGS0=101P CGD0=4P CBD=66.2P PB=1

.MODEL DIODE1 D IS=5.516E-13 RS=0.2084 N=1.0078

.ENDS ZVN4424

For clarification of the above or for technical enquires generally please contact the Applications Dept. at Zetex plc.

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